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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,520	08/04/2003	Matthew J. Gilbert	05-796-US	9012

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EXAMINER	
PATEL, NIRAV B	
ART UNIT	PAPER NUMBER
2135	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/634,520	GILBERT ET AL.	
	Examiner	Art Unit	
	NIRAV PATEL	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,35 and 39-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,35 and 39-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/18/05, 5/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the communication filed on 1/21/2008.

2. Claims 1-24, 35, 39-43 are pending. Applicant's election without traverse of the elected group Species I, claims 1-24, 35, 39-43, in the reply filed on 1/21/08 is acknowledged. Claims 25-34, 36-38, 44-53 are withdrawn and canceled by the applicant from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group II, III IV.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by del Alamo et al. (US Patent No. 5,105,232).

As per claim 1, del Alamo teaches:

A quantum gate comprising two waveguides [Fig. 2], an input section of at least one of the waveguides leading to a coupling region where the two waveguides are coupled, an output section of each of the waveguides leading from the coupling region to an output end of the waveguide [Fig. 2, 3], and at least one bias element operative to apply one of an electrical and magnetic bias to the gate to cause carriers moving through the input section of the at least one waveguide into the coupling region to be coupled to one or the other of the output sections of the waveguides in dependence on application of the bias [Fig. 2, 3, col. 2 lines 64-68, col. 3 lines 1-7, 30-49, col. 1 lines 9-16].

As per claim 2, the rejection of claim 1 is incorporated and del Alamo teaches:

the coupling region is a tunneling region for passing carriers from the at least one waveguide to the other waveguide by tunneling [Fig. 2, 3, col. 3 lines 30-68, col. 4 lines 1-4, Fig. 5, 6].

As per claim 3, the rejection of claim 1 is incorporated and del Alamo teaches:

wherein the at least one bias element is operative to apply an electrical bias across the gate to force carrier movement across the coupling region from the input section of the at least one waveguide to one or the other of the output sections [Fig. 2, 3, col. 3 lines 30-68, col. 4 lines 1-4, Fig. 5, 6].

As per claim 4, the rejection of claim 1 is incorporated and del Alamo teaches:

wherein the at least one bias element is operative to apply a magnetic bias to the gate to force carrier movement across the coupling region from the input of the at least one waveguide to one or the other of the output sections [Fig. 2, 3, col. 3 lines 30-68, col. 4 lines 1-4, Fig. 5, 6].

As per claim 5, the rejection of claim 4 is incorporated and del Alamo teaches:

wherein the bias element is a conductor proximate the coupling region [Fig. 1, 2, 3].

As per claim 6, the rejection of claim 1 is incorporated and del Alamo teaches:

the waveguides and the coupling region are a part of a semiconductor structure [Fig. 1, 2, 3].

As per claim 7, the rejection of claim 6 is incorporated and del Alamo teaches:

the semiconductor structure being of a InAs/InGaAs heterostructure [Fig. 1-3, col. 6 lines 60-68].

As per claim 8, the rejection of claim 1 is incorporated and del Alamo teaches:

the at least one waveguide is of substantially uniform width and the other waveguide has an output region that is wider than the width of the at least one waveguide [Fig. 1, 2, 3].

As per claim 9, the rejection of claim 6 is incorporated and del Alamo teaches:

wherein the other waveguide has an input region leading to the coupling region that is narrower than the output region of that waveguide [Fig. 1-3].

As per claim 10, the rejection of claim 1 is incorporated and del Alamo teaches:

wherein the coupling region is 300 to 450 nm in length [col. 5 lines 1-68].

As per claim 11, the rejection of claim 10 is incorporated and del Alamo teaches:

wherein the waveguides are 20 to 50 nm in width [col. 5 lines 1-68].

As per claim 12, the rejection of claim 1 is incorporated and del Alamo teaches:

the waveguides are separated by a potential barrier at locations other than the coupling region [Fig. 7, 9, col. 5 lines 25-53].

As per claim 13, the rejection of claim 9 is incorporated and del Alamo teaches:

wherein the input and output regions of the waveguides are separated by a potential barrier [Fig. 7, 9, col. 5 lines 25-53].

As per claim 14, the rejection of claim 12 is incorporated and del Alamo teaches:

the potential barriers comprise deposited conductors [Figs. 1-3].

As per claim 15, the rejection of claim 12 is incorporated and del Alamo teaches:

potential barriers defining edges of the waveguides spaced from the potential barriers separating the waveguides [col. 5 lines 25-68, col. 6 lines 1-8].

As per claim 16, the rejection of claim 15 is incorporated and del Alamo teaches:

the potential barriers comprise deposited conductors [Figs. 1-3].

As per claim 17, the rejection of claim 13 is incorporated and del Alamo teaches:

potential barriers defining edges of the waveguides spaced from the potential barriers separating the waveguides [col. 5 lines 25-68, col. 6 lines 1-8].

As per claim 18, the rejection of claim 17 is incorporated and del Alamo teaches:

the potential barriers comprise deposited conductors [Figs. 1-3].

As per claim 19, the rejection of claim 1 is incorporated and del Alamo teaches:

means associated with the input region of the at least one waveguide operative to modify a quantum characteristic of charge carriers moving in that input region towards the coupling region [Fig. 1-3, col. 5 lines 26-68, col. 6 lines 1-15].

As per claim 20, the rejection of claim 19 is incorporated and del Alamo teaches:

the quantum characteristic is electron spin, whereby carriers moving in the input region of the at least waveguide are selectively electron spin polarized by operation of the means to modify a quantum characteristic [Fig. 1-3, col. 5 lines 26-68, col. 6 lines 1-15].

As per claim 21, the rejection of claim 19 is incorporated and del Alamo teaches:

the quantum characteristic is electron spin and wherein the means to modify a quantum characteristic is a quantum point contact (QPC) and a source of magnetic field associated with the input region of the at least one waveguide [col. 5 lines 26-68, col. 6 lines 1-15, Fig. 4-8].

As per claim 22, the rejection of claim 1 is incorporated and del Alamo teaches:

a quantum point contact and a source of magnetic field associated with the input region of the at least one waveguide operative selectively to effect electron spin polarization of carriers moving in that input region [col. 5 lines 26-68, col. 6 lines 1-15, Fig. 3-8].

As per claim 23, the rejection of claim 1 is incorporated and del Alamo teaches:

the charge carriers are electrons [col. 4 lines 19-54].

As per claim 24, the rejection of claim 1 is incorporated and del Alamo teaches:

the waveguides are defined by deposited metal conductors operative to develop potential barriers in a semiconductor substrate on which they are deposited and in which the charge carriers move [Fig. 1-3, col. 5 lines 24-54].

4. Claims 35, 39-43 are rejected under 35 U.S.C. 102(b) as being anticipated by del Alamo et al. (US Patent No. 5,105,232).

As per claim 35, Inai teaches: A semiconductor waveguide gate device comprising [Fig. 1]: (a) a first waveguide boundary, (b) a second waveguide boundary spaced from and substantially parallel to the first waveguide boundary [Fig. 1, 14], (c) a first metallic member defining a first waveguide separating boundary protruding between the first waveguide boundary and the second waveguide boundary, (d) a second metallic member defining a second waveguide separating boundary protruding towards the first electrode between the first waveguide boundary and the second waveguide boundary [Fig. 14], (e) each of the first and second metallic members having edges facing the first waveguide boundary to define a potential barrier spaced substantially the same distance a from the first waveguide boundary [Fig. 1], (f) each of the first and second metallic members having a further edge facing the second waveguide boundary [Fig. 2, 6], (i) the further edge of the first metallic member being spaced from the second waveguide boundary to produce a potential barrier a distance b from the second waveguide boundary [Fig.1, 2, 9, 10, 12, 14], (ii) the further edge of the second metallic member being spaced from the second waveguide to produce a potential barrier a distance c from the second waveguide boundary that is greater than a [Fig.1, 2, 9, 10, 12, 14], (iii) the further potential barriers of the first and second metallic members forming with the second waveguide boundary a second waveguide along the second waveguide boundary [Fig.1, 2, 9, 10, 12, 14], (g) the first and second metallic members having ends separated by a coupling [Fig.1, 2, 9, 10, 12, 14], and (h) bias applying means located to selectively apply one of a magnetic and an electrical bias to charged particles moving in the first and second waveguides [Fig. 3, 4].

As per claim 39, Inai teaches:

A method of transistor quantum gate operation comprising: (a) providing in a semiconductor substrate a first waveguide [Fig. 1], (b) providing in the semiconductor substrate a second waveguide [Fig. 2, 14], (c) providing a coupling between the first and the second waveguide [Fig. 1, 11, 14], (d) moving a charge carrier current in one of the waveguides [Fig. 2, 5, 6], and (e) selectively controlling the path of electron current to one or the other of outputs of the waveguides by applying at least one of an electrical and a magnetic bias to the electron current to cause tunneling of the current in the coupling [Fig. 2-4, 6-8].

As per claim 40, the rejection of claim 39 is incorporated and Inai teaches:

steps (a) and (b) comprise developing barrier potentials in the substrate to define the waveguides [Fig. 1, 11, 12, 24-26].

As per claim 41, the rejection of claim 40 is incorporated and Inai teaches:

wherein developing the barrier potentials comprises: (i) developing a first barrier potential separating the waveguides at their input ends between inputs to the waveguides and the coupling, and (ii) developing a second barrier potential separating the waveguides at their output ends between outputs from the waveguides and the coupling [Fig. 1, 2, 6].

As per claim 42, the rejection of claim 41 is incorporated and Inai teaches:

wherein developing the first and second barrier potentials comprises defining one waveguide that is wider at its output end than width of the other waveguide at its input end [Fig. 9, 10, 24-26, 27, 28].

As per claim 43, the rejection of claim 39 is incorporated and Inai teaches:

selectively polarizing the electron spin of charge carriers moved in one of the waveguides [Fig. 1, 2, 6].

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Taylor et al (US 5,329,137) --- integrated total internal reflection optical switch utilizing charge storage in a quantum well

Saito (US 5283445) – Quantum Semiconductor device employing quantum boxes for enabling compact size and high-speed operation

Deliwala (US 6690844) – Optical fiber apparatus and associated method

Lorenzo et al (US 4877299) -- Metal-insulator-semiconductor control of guided optical waves in semiconductor waveguides

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIRAV PATEL whose telephone number is (571)272-5936. The examiner can normally be reached on 8 am - 4:30 pm (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on 571-272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from

either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NBP
4/1/08

/KIMYEN VU/

Supervisory Patent Examiner, Art Unit 2135